What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

setting a row line and a column line associated with said memory element to respective voltage levels such that no current flows through said memory element;

changing the voltage at one of said row line and said column line to a level sufficient to initiate current flow through said memory element; and

comparing the voltage on the one of said row line and said column line that is being discharged with a reference voltage to determine a logical state of said memory element.

2. The method of claim 1, wherein said act of setting comprises setting said row line and said column line to a common voltage level.

3. The method of claim 1, wherein said act of setting comprises setting a plurality of row lines and a plurality of column lines in a memory array with which said memory element is associated to a common voltage level.

4. The method of claim 1, wherein said act of changing comprises changing the voltage at said row line to approximately zero volts.

5. The method of claim 2 further comprising discharging a voltage level at one of said row line and said column line through said memory element and an isolation diode.

6. The method of claim 5, wherein said act of setting comprises setting said row line and said column line to a voltage level approximately equal to a threshold voltage of said diode plus an additional voltage sufficient to enable a read operation of said memory element.

7. The method of claim 1, wherein said act of setting comprises precharging said row line and said column line to said respective voltage levels.

8. The method of claim 2, wherein said act of setting comprises precharging said row line and said column line to said common voltage.

9. The method of claim 8 further comprising equilibrating said voltage on said row line and said column line.

10. The method of claim 1, wherein said act of changing comprises changing said voltage level at one of said row line and said column line such that a potential voltage difference across a programmable conductor memory cell containing said programmable conduct memory element is at least equal to a threshold voltage of an isolation diode of said memory cell coupled to said programmable conductor memory element plus a voltage sufficient to enable a read operation of said memory element.

11. The method of claim 1, wherein said act of comparing comprises discharging a voltage level, at the one of said row line and said column line that did not change, through said memory element.

12. The method of claim 1, wherein said act of comparing comprises comparing a voltage at said column line with said reference voltage a predetermined time after said act of changing.

13. The method of claim 1, wherein said act of comparing comprises comparing a voltage level at said column line with said reference voltage in order to determine said logical state.

14. The method of claim 2 further comprising discharging a voltage level at one of said row line and said column line through said memory element and a zener diode.

15. The method of claim 14, wherein said act of setting comprises setting said row line and said column line to a voltage level approximately equal to a threshold voltage of said zener diode plus an additional voltage sufficient to enable a read operation of said memory element.

16. The method of claim 1, wherein said act of changing comprises changing said voltage at one of said row line and said column line in order to have a voltage potential difference across said memory element sufficient to read said logical state, but insufficient to program said memory element.

17. The method of claim 1 further comprising reading a high resistance level for said programmable conductor memory element.

18. The method of claim 1 further comprising reading a low resistance level for said programmable conductor memory element.

19. The method of claim 18 further comprising reprogramming said low resistance level into said memory element.

20. The method of claim 19, wherein said act of reprogramming comprises raising a voltage at one of said column line and said row line to a level sufficient to place a programming voltage across said memory element sufficient to program said element to a low resistance state.

21. A method of sensing a stored value of a programmable conductor random access memory element, the method comprising:

setting a plurality of row lines and a plurality of column lines associated with a memory array to a common voltage such that no current flows through said memory element;

changing the voltage at a selected row line to approximately zero volts such that a current flow is initiated from a column line associated with said memory element through said memory element and through a diode circuit coupled to said memory element; and

comparing the voltage at said column line with a reference voltage a predetermined time after said act of changing in order to determine a logical state of said memory element.

22. The method of claim 21, wherein said act of changing comprises changing the voltage at a selected row line to approximately zero volts such that current flow is initiated from a column line associated with said memory element through said memory element and through a reverse connected diode pair coupled to a said memory element.

23. The method of claim 21, wherein said act of changing comprises changing the voltage at a selected row line to approximately zero volts such that current flow is initiated from a column line associated with said memory element through said memory element and through a zener diode coupled to a said memory element.

24. A method of sensing a stored value of a programmable conductor random access memory cell, the method comprising:

setting a column line and a row line associated with said memory cell to a common voltage level;

reducing said voltage at said row line to a level such that a diode circuit coupled to a programmable conductor memory element of said cell is activated and such that a voltage potential difference across said memory element is sufficient to read a logical state of said memory element, but insufficient to program said memory element.

25. The method of claim 24, wherein said act of reducing comprises reducing said voltage at said row line to a level such that a reverse connected diode pair coupled to said programmable conductor memory element of said memory cell is activated.

26. The method of claim 24, wherein said act of reducing comprises reducing said voltage at said row line to a level such that a zener diode coupled to said programmable conductor memory element of said memory cell is activated.

27. A semiconductor memory structure, comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first terminal of a diode circuit, wherein

a second terminal of said diode circuit is coupled to said row line; and

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.

28. The structure of claim 27 further comprising precharge circuits for respectively precharging said column line and said row line to a common predetermined voltage level prior to said read operation.

29. The structure of claim 28 further comprising equilibrate circuits for respectively equilibrating voltages at said column line and said row line to said common predetermined voltage.

30. The structure of claim 28, wherein said common predetermined voltage is approximately equal to a threshold voltage of said diode circuit plus an additional voltage sufficient to read said logical state of said programmable conductor memory element.

31. The structure of claim 27, wherein said programmable conductor memory element comprises a chalcogenide glass having first and second electrodes.

32. The structure of claim 31, wherein said chalcogenide glass has a Ge:Se glass composition which is doped with Ag.

33. The structure of claim 27, wherein said diode circuit comprises a reverse connected diode pair.

34. The structure of claim 27, wherein said diode circuit comprises a zener diode.

35. The structure of claim 27 further comprising a switch between said row line and said precharge circuit for switchably coupling said row line to said precharge circuit before said read operation.

36. A processor system, comprising:

a processor; and

a semiconductor memory structure coupled to said processor, said semiconductor memory structure comprising:

a column line and a row line associated with a programmable conductor random access memory cell;

a programmable conductor memory element, a first terminal of which is coupled to said column line and a second terminal of which is coupled to a first terminal of a diode circuit, wherein

a second terminal of said diode circuit is coupled to said row line; and

a sense amplifier for comparing a voltage on said column line with a reference voltage during a read operation to determine a logical state of said programmable conductor memory element.

37. The system of claim 36, wherein said semiconductor memory structure further comprises precharge circuits for respectively precharging said column line and said row line to a common predetermined voltage level prior to said read operation.

38. The system of claim 37, wherein said semiconductor memory structure further comprises equilibrate circuits for respectively equilibrating voltages at said column line and said row line to said common predetermined voltage.

39. The system of claim 37, wherein said common predetermined voltage is approximately equal to a threshold voltage of said diode circuit plus an additional voltage sufficient to read said logical state of said programmable conductor memory element.

40. The system of claim 36, wherein said programmable conductor memory element comprises a chalcogenide glass having first and second electrodes.

41. The system of claim 40, wherein said chalcogenide glass has a Ge:Se glass composition which is doped with Ag.

42. The system of claim 36, wherein said diode circuit comprises a reverse connected diode pair.

43. The system of claim 36, wherein said diode circuit comprises a zener diode.

44. The system of claim 36, wherein said semiconductor memory structure further comprises a switch between said row line and said precharge circuit for switchably coupling said row line to said precharge circuit before said read operation.